5   **CLAIMS**

What is claimed is:

1   1. A method for detecting biphase encoded data comprising:

2   receiving a biphase encoded signal, the biphase encoded signal characterized as

3   including unit bit cells each having a logic value encoded as a mid-symbol signal

4   transition between a first half-symbol signal component and a second half-symbol signal

5   component;

6   demodulating the first and second half-symbol signal components of a unit bit

7   cell; and

8   generating a difference signal corresponding to the difference between the

9   demodulated first and second half-symbol components, such that the difference signal

10   may be utilized to determine the logic value of the unit bit cell.

1   2. The method of claim 1, further comprising detecting the logic value of the received

2   unit bit cell by comparing the difference signal with a validity threshold value.

1   3. The method of claim 1, wherein the received biphase encoded signal is a Manchester

2   encoded signal.

1   4. The method of claim 1, wherein said biphase encoded signal is modulated as

2   amplitude shift keyed, frequency shift keyed, or phase shift keyed.

1   5. The method of claim 1, wherein said step of generating a difference signal comprises

2   subtracting the demodulated first half-symbol signal component from the demodulated

3   second half-symbol signal component.

1   6. The method of claim 1, wherein said step of generating a difference signal comprises

2   subtracting the demodulated second half-symbol signal component from the demodulated

3   first half-symbol signal component.

1   7. The method of claim 1, said demodulating step comprising demodulating the first and

2   second half-symbol signal components of the unit bit cell over sequential half symbol

3   clock periods.

1   8. The method of claim 1, wherein said demodulating step further comprising correlating

2   the first and second half-symbol signal components of the unit bit cell.

1   9. The method of claim 8, wherein said correlating step comprises separating the first

2   and second half-symbol signal components of the unit bit cell.

1   10. The method of claim 8, said demodulating step further comprising integrating the

2   correlated first and second half-symbol signal components of the unit bit cell.

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1   11. A biphase code detector for detecting biphase encoded data comprising:

2   a receiver that receives a biphase encoded signal, wherein the biphase encoded

3   signal is characterized as including unit bit cells each having a logic value encoded as a

4   mid-symbol transition between a first half-symbol signal component and a second half-

5   symbol signal component;

6   a demodulator that demodulates the first and second half-symbol components; and

7   a half-symbol differentiator that generates a difference signal corresponding to the

8   difference between the demodulated first and second half-symbol components, such that

9   the difference signal may be utilized to determine the logic value of the unit bit cell.

1   12. The system of claim 11, further comprising an output detector that compares the

2   difference signal with a validity threshold value to determine the logic value of the

3   received unit bit cell.

1   13. The system of claim 11, wherein said half-symbol differentiator comprises a

2   subtractor.

1   14. The system of claim 11, said demodulator further comprising means for correlating

2   the first and second half-symbol components over sequential half-symbol clock periods.

1   15. The system of claim 14, wherein said correlation means comprises a first and a

2   second integrate and dump circuit.

1   16. The system of claim 15, wherein said correlation means further comprises:

2   means for separating and passing the first half-symbol component to either the

3   first or second integrate and dump circuit; and

4   means for separating and passing the second half-symbol component to the other

5   of the first or second integrate and dump circuits.

1   17. The system of claim 16, wherein said means for separating and passing comprise

2   correlation multipliers.

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